Quiz #3

May 28, 2007
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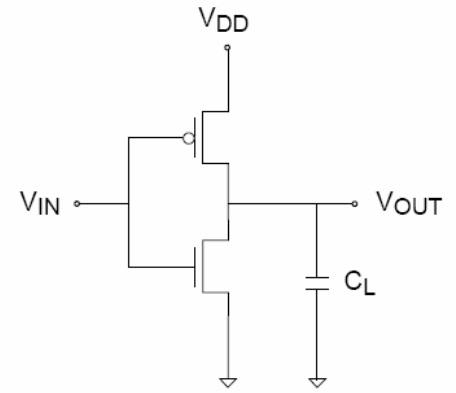
Electronic Circuits II

Problem 1 (4)

Consider the following CMOS inverter having v_{Tn}=1V, v_{Tp}= -1V, V_{DD} = 2.5V, r_{on} = r_{op} = 50KΩ, and k'(W/L)=1mA/V^2 for both NMOS and PMOS transistors,



Estimate the noise margin for the low logic level.

Problem 2 (3)

Draw the transistor-level circuit configuration for CMOS XOR gate. Assume the input signals are available in A, A, B and B.

Problem 3 (3)

Consider the following block diagram for PLL.
Assume the phase detector has gain of K_{PD}, the VCO has gain of K_{VCO}, and the low pass filter has one pole at ω_p. Derive the close-loop transfer function in s-domain for ϕ_{out}/ϕ_{in}.